What Is Claimed Is:

1. A method for forming a conductive wire of a semiconductor device, comprising:

etching a lower portion of a side wall of a silicon layer pattern based on a difference of etching selectivities between a silicon layer and a lower film; and

forming a T-shaped conductive wire based on the silicon layer pattern.

2. The method of claim 1, wherein the lower layer comprises an insulating material, wherein the etching selectivity of the insulating material to that of the silicon layer is 1:5 to 500.

3. A method for forming conductive wires of a semiconductor device, comprising the steps of:

forming a first interlayer insulating film on a semiconductor substrate having a lower metal wire;

forming a diffusion barrier layer over the resulting structure;

forming a sacrificial conductive layer on the diffusion barrier layer;

forming a T-shaped sacrificial conductive layer pattern based on a photolithography process using an upper metal wire mask to etch a lower portion of a side wall of a sacrificial conductive layer by utilizing a notching phenomenon;

forming a planarized second interlayer insulating film exposing the sacrificial conductive layer on the entire surface, the second interlayer dielectric film filling an under-cut of the T-shaped sacrificial conductive layer pattern;

removing the sacrificial conductive layer pattern by etching an exposed portion of the diffusion barrier layer to simultaneously form a via contact hole and a trench

exposing the lower metal wiring; and

forming an upper metal wire connected to the lower metal wire by filling the via contact hole and the trench.

4. The method of claim 3, wherein the sacrificial conductive layer comprises silicon.

5. The method of claim 3, wherein the sacrificial conductive layer comprises an amorphous silicon layer having a thickness of 5000 to 12000Å formed by a chemical vapor deposition process at a temperature ranging from 50 to 350℃.

6. The method of claim 3, wherein the sacrificial conductive layer comprises a polysilicon layer having a thickness of 5000 to 12000Å formed by a chemical vapor deposition process at a temperature ranging from 300 to 850℃.

7. The method of claim 3, wherein a ratio of etching selectivity of the diffusion barrier layer to that of the sacrificial conductive layer is approximately 1 : 5 to 500.

8. The method of claim 7, wherein the diffusion barrier layer comprises at least one of Si_3N_4 and SiC, and wherein the sacrificial conductive layer comprises at least one of amorphous silicon and low temperature polysilicon, formed by a chemical vapor deposition process.

9. The method of claim 3, wherein the etching process of the sacrificial

conductive layer is a dry etching process using an etching gas comprising a halogen, and a supplementary etching gas selected from a group consisting of N_2, O_2, Ar, He, Ne, and Kr.

10. The method of claim 9, wherein the etching gas is selected from a group consisting of C_xF_y gas, Cl_2 gas, and HBr gas.

11. The method of claim 3, wherein the second interlayer insulating film comprises at least one of an oxide film comprising hydrogen or fluorine, and an organic chemical material with a low viscosity and dielectric coefficient.

12. The method of claim 3, wherein the step of removing the sacrificial conductive layer pattern is a dry etching process based on a different etching selectivity between the sacrificial conductive layer pattern and the second interlayer dielectric film.

13. The method of claim 12, wherein the dry etching process uses a gas selected from a group consisting of C_xF_y gas, Cl_2 gas, and HBr.

14. The method of claim 3, wherein the step of removing the sacrificial conductive layer pattern is a wet etching process using acetic acid or nitric acid, and is based on a different etching selectivity between the sacrificial conductive layer pattern and the second interlayer dielectric film.